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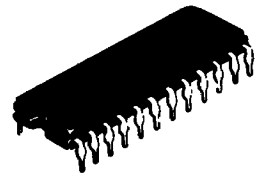
## 2048-word x 8-bit High Speed CMOS Static RAM

Jameco Part Number 42737

### ■FEATURES

- Single 5V Supply
- High speed: Fast Access Time 120ns/150ns/200ns (max.)
- Low Power Standby and Low Power Operation
  - Standby: 100μW (typ.)
    10μW (typ.) (L-version)
  - Operation: 200mW (typ.)
    175mW (typ.) (L-version)
- Completely Static RAM: No clock or Timing Strobe Required
- Directly TTL Compatible: All Input and Output
- Pin Out Compatible with Standard 16K EPROM/MASK ROM
- Equal Access and Cycle Time
- Capability of Battery Back Up Operation (L-version)

HM6116P Series



(DP-24)

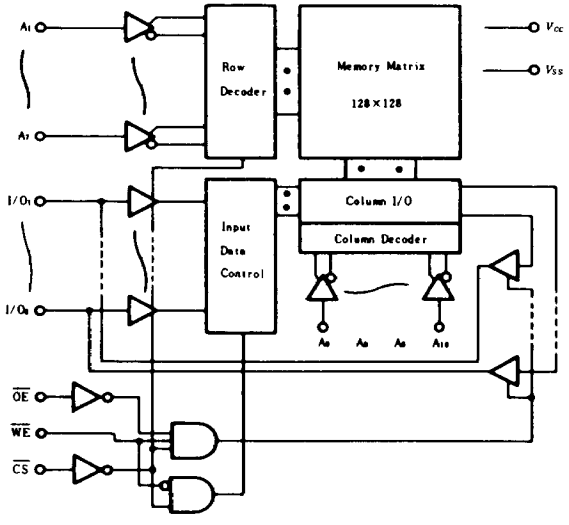
HM6116FP Series

(FP-24D)

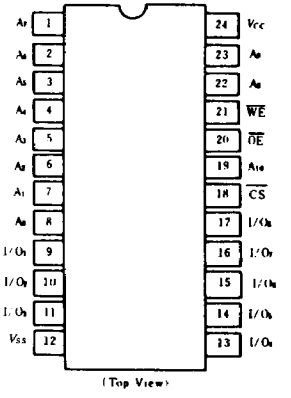
### ■ORDERING INFORMATION

| Type No. | Access Time | Package |
|---|---|---|
| HM6116P-2<br>HM6116P-3<br>HM6116P-4 | 120ns<br>150ns<br>200ns | 600mil 24pin Plastic DIP |
| HM6116LP-2<br>HM6116LP-3<br>HM6116LP-4 | 120 ns<br>150 ns<br>200 ns | |
| HM6116FP-2<br>HM6116FP-3<br>HM6114FP-4 | 120 ns<br>150 ns<br>200 ns | 24pin Plastic SOP |
| HM6116LFP-2<br>HM6116LFP-3<br>HM6116LFP-4 | 120 ns<br>150 ns<br>200 ns | |

### ■FUNCTIONAL BLOCK DIAGRAM




### ■PIN ARRANGEMENT




**Note) This device is not available for new application.**



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## ■ABSOLUTE MAXIMUM RATINGS

| Item | Symbol | Rating | Unit |
|---|---|---|---|
| Voltage on Any Pin Relative to $V_{SS}$ | $V_T$ | −0.5*1 to +7.0 | V |
| Operating Temperature | $T_{opr}$ | 0 to +70 | °C |
| Storage Temperature | $T_{stg}$ | −55 to +125 | °C |
| Storage Temperature Under Bias | $T_{bias}$ | −10 to +85 | °C |
| Power Dissipation | $P_T$ | 1.0 | W |

Note) *1. −3.5V for pulse width≦50ns

## ■TRUTH TABLE

| $\overline{CS}$ | $\overline{OE}$ | $\overline{WE}$ | Mode | $V_{CC}$ Current | I/O Pin | Ref. Cycle |
|---|---|---|---|---|---|---|
| H | × | × | Not Selected | $I_{SB}$, $I_{SB1}$ | High Z | |
| L | L | H | Read | $I_{CC}$ | Dout | Read Cycle (1)~(3) |
| L | H | L | Write | $I_{CC}$ | Din | Write Cycle (1) |
| L | L | L | Write | $I_{CC}$ | Din | Write Cycle (2) |

## ■RECOMMENDED DC OPERATING CONDITIONS ($Ta$=0 to +70°C)

| Item | Symbol | min | typ | max | Unit |
|---|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 4.5 | 5.0 | 5.5 | V |
| | $V_{SS}$ | 0 | 0 | 0 | V |
| Input Voltage | $V_{IH}$ | 2.2 | 3.5 | 6.0 | V |
| | $V_{IL}$ | −0.3*1 | — | 0.8 | V |

Note) *1. −3.0V for pulse width≦50ns.

## ■DC AND OPERATING CHARACTERISTICS ($V_{CC}$=5V±10%, $V_{SS}$=0V, $Ta$=0 to +70°C)

| Item | Symbol | Test Conditions | HM6116-2 | | | HM6116-3/-4 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | min | typ*1 | max | min | typ*1 | max | |
| Input Leakage Current | $\|I_{LI}\|$ | $V_{CC}$=5.5V, $V_{IN}$=$V_{SS}$ to $V_{CC}$ | — | — | 10 | — | — | 10 | μA |
| | | | — | — | 2*3 | — | — | 2*3 | |
| Output Leakage Current | $\|I_{LO}\|$ | $\overline{CS}$=$V_{IH}$ or $\overline{OE}$=$V_{IH}$, $V_{I/O}$=$V_{SS}$ to $V_{CC}$ | — | — | 10 | — | — | 10 | μA |
| | | | — | — | 2*3 | — | — | 2*3 | |
| Operating Power Supply Current | $I_{CC}$ | $\overline{CS}$=$V_{IL}$, $I_{I/O}$=0mA | — | 40 | 80 | — | 35 | 70 | mA |
| | | | — | 35*3 | 70*3 | — | 30*3 | 60*3 | |
| | $I_{CC1}$*2 | $V_{IH}$=3.5V, $V_{IL}$=0.6V, $I_{I/O}$=0mA | — | 35 | — | — | 30 | — | mA |
| | | | — | 30*3 | — | — | 25*3 | — | |
| Average Operating Current | $I_{CC2}$ | Min. cycle, duty=100% $I_{I/O}$=0mA | — | 40 | 80 | — | 35 | 70 | mA |
| | | | — | 35*3 | 70*3 | — | 30*3 | 60*3 | |
| Standby Power Supply Current | $I_{SB}$ | $\overline{CS}$=$V_{IH}$ | — | 5 | 15 | — | 5 | 15 | mA |
| | | | — | 4*3 | 12*3 | — | 4*3 | 12*3 | |
| | $I_{SB1}$ | $\overline{CS}$≧$V_{CC}$−0.2V, 0V≦$V_{IN}$≦0.2V or $V_{CC}$−0.2V≦$V_{IN}$ | — | 0.02 | 2 | — | 0.02 | 2 | μA |
| | | | — | 2*3 | 50*3 | — | 2*3 | 50*3 | |
| Output Voltage | $V_{OL}$ | $I_{OL}$=4mA | — | — | 0.4 | — | — | — | V |
| | | $I_{OL}$=2.1mA | — | — | — | — | — | 0.4 | V |
| | $V_{OH}$ | $I_{OH}$=−1.0mA | 2.4 | — | — | 2.4 | — | — | V |

Notes) *1. $V_{CC}$=5V, $Ta$=25°C
*2. Reference Only
*3. This characteristics are guaranteed only for L-version.



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## ■CAPACITANCE ($f$=1MHz, $Ta$=25°C)

| Item | Symbol | Test Conditions | typ | max | Unit |
|---|---|---|---|---|---|
| Input Capacitance | $C_{in}$ | $V_{in}$=0V | 3 | 5 | pF |
| Input/Output Capacitance | $C_{I/O}$ | $V_{I/O}$=0V | 5 | 7 | pF |

Note) This parameter is sampled and not 100% tested.

## ■AC CHARACTERISTICS ($V_{CC}$=5V±10%, $Ta$=0 to +70°C)

### ●AC TEST CONDITIONS

Input Pulse Levels: 0.8 to 2.4V
Input Rise and Fall Times: 10 ns
Input and Output Timing Reference Levels: 1.5V
Output Load: 1TTL Gate and $C_L$ (100pF) (including scope and jig)

### ●READ CYCLE

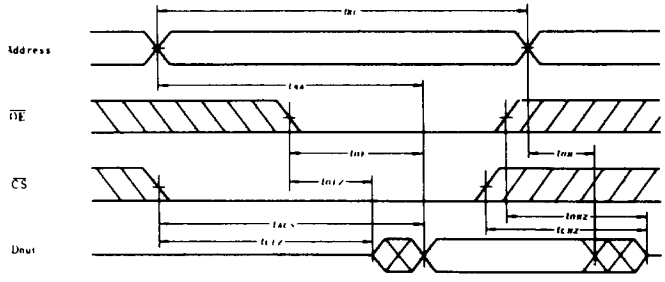
| Item | Symbol | HM6116-2 | | HM6116-3 | | HM6116-4 | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | min | max | min | max | min | max | |
| Read Cycle Time | $t_{RC}$ | 120 | — | 150 | — | 200 | — | ns |
| Address Access Time | $t_{AA}$ | — | 120 | — | 150 | — | 200 | ns |
| Chip Select Access Time | $t_{ACS}$ | — | 120 | — | 150 | — | 200 | ns |
| Chip Selection to Output in Low Z | $t_{CLZ}$ | 10 | — | 15 | — | 15 | — | ns |
| Output Enable to Output Valid | $t_{OE}$ | — | 80 | — | 100 | — | 120 | ns |
| Output Enable to Output in Low Z | $t_{OLZ}$ | 10 | — | 15 | — | 15 | — | ns |
| Chip Deselection to Output in High Z | $t_{CHZ}$ | 0 | 40 | 0 | 50 | 0 | 60 | ns |
| Chip Disable to Output in High Z | $t_{OHZ}$ | 0 | 40 | 0 | 50 | 0 | 60 | ns |
| Output Hold from Address Change | $t_{OH}$ | 10 | — | 15 | — | 15 | — | ns |

### ●WRITE CYCLE

| Item | Symbol | HM6116-2 | | HM6116-3 | | HM6116-4 | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | min | max | min | max | min | max | |
| Write Cycle Time | $t_{WC}$ | 120 | — | 150 | — | 200 | — | ns |
| Chip Selection to End of Write | $t_{CW}$ | 70 | — | 90 | — | 120 | — | ns |
| Address Valid to End of Write | $t_{AW}$ | 105 | — | 120 | — | 140 | — | ns |
| Address Set Up Time | $t_{AS}$ | 20 | — | 20 | — | 20 | — | ns |
| Write Pulse Width | $t_{WP}$ | 70 | — | 90 | — | 120 | — | ns |
| Write Recovery Time | $t_{WR}$ | 5 | — | 10 | — | 10 | — | ns |
| Output Disable to Output in High Z | $t_{OHZ}$ | 0 | 40 | 0 | 50 | 0 | 60 | ns |
| Write to Output in High Z | $t_{WHZ}$ | 0 | 50 | 0 | 60 | 0 | 60 | ns |
| Data to Write Time Overlap | $t_{DW}$ | 35 | — | 40 | — | 60 | — | ns |
| Data Hold from Write Time | $t_{DH}$ | 5 | — | 10 | — | 10 | — | ns |
| Output Active from End of Write | $t_{OW}$ | 5 | — | 10 | — | 10 | — | ns |

## ■TIMING WAVEFORM

### ●READ CYCLE (1)[1]



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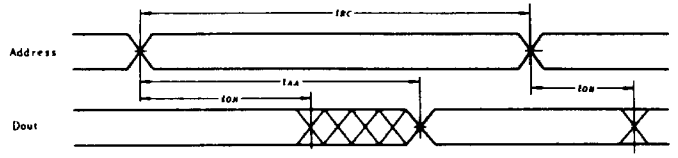
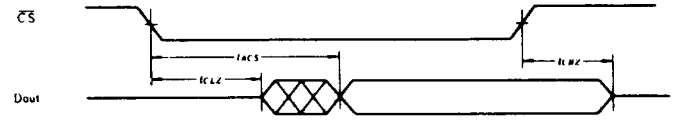
● **READ CYCLE (2)** [1][2][4]

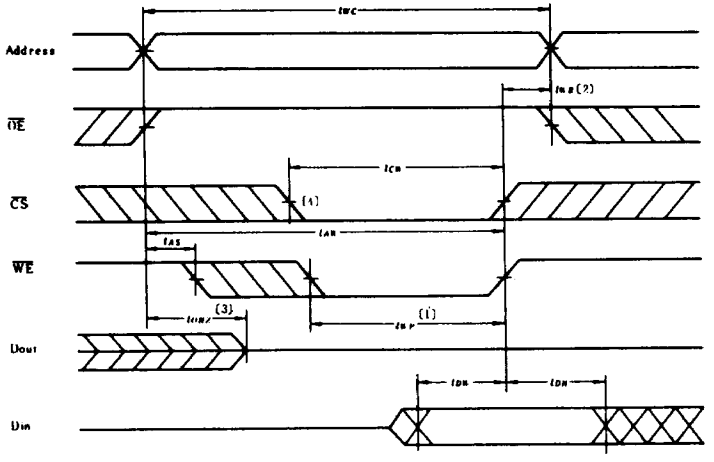



● **READ CYCLE (3)** [1][3][4]




NOTES: 1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS} = V_{IL}$.
3. Address Valid prior to or coincident with $\overline{CS}$ transition Low.
4. $\overline{OE} = V_{IL}$.

● **WRITE CYCLE (1)**



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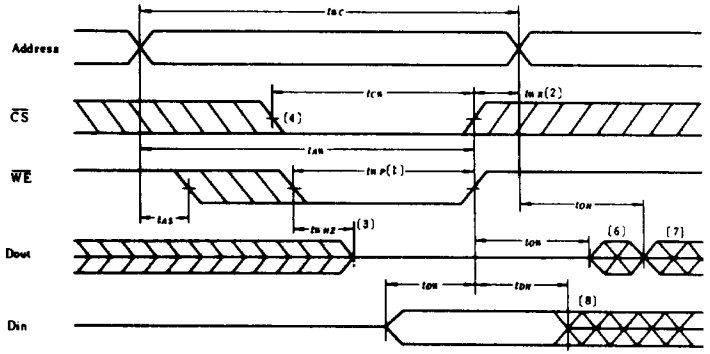
## ●WRITE CYCLE (2)[5]




NOTES:
1. A write occurs during the overlap ($t_{WP}$) of a low $\overline{CS}$ and a low $\overline{WE}$.
2. $t_{WR}$ is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, output remain in a high impedance state.
5. $\overline{OE}$ is continuously low. ($\overline{OE} = V_{IL}$)
6. $D_{out}$ is the same phase of write data of this write cycle.
7. $D_{out}$ is the read data of next address.
8. If $\overline{CS}$ is Low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.

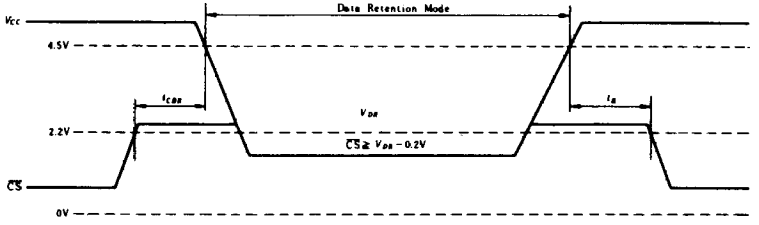
## ■LOW Vcc DATA RETENTION CHARACTERISTICS ($Ta = 0$ to $+70°C$)

This characteristics are guaranteed only for L-version.

| Item | Symbol | Test Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ for Data Retention | $V_{DR}$ | $\overline{CS} \geq V_{CC} - 0.2V$, $V_{in} \geq V_{CC} - 0.2V$ or $V_{in} \leq 0.2V$ | 2.0 | — | — | V |
| Data Retention Current | $I_{CCDR}$ *1 | $V_{CC} = 3.0V$, $\overline{CS} \geq 2.8V$, $V_{IH} \geq 2.8V$ or $0V \leq V_{IN} \leq 0.2V$ | — | — | 30 | μA |
| Chip Deselect to Data Retention Time | $t_{CDR}$ | See Retention Waveform | 0 | — | — | ns |
| Operation Recovery Time | $t_R$ | | $t_{RC}$ *2 | — | — | ns |

Notes) *1. 10μA max at $Ta = 0°C$ to $+40°C$, $V_{IL}$ min $= -0.3V$
*2. $t_{RC}$ = Read Cycle Time.

### ●Low Vcc Data Retention Waveform



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